CLAIMS

1. A verification system controlled by a master clock for verifying the proper operation of a user circuit design, comprising:

reception logic for receiving input data to be evaluated within an evaluation time;

evaluation logic for modeling the user circuit design in reconfigurable hardware logic and evaluating the input data during the evaluation time; and

clock generation logic for generating a plurality of asynchronous clocks for use by the evaluation logic and controlling the phase relationship among the plurality of asynchronous clocks.

2. The system of claim 1, wherein the reconfigurable hardware logic in the evaluation logic includes at least one reconfigurable hardware logic chip.

3. The system of claim 2, wherein the reconfigurable hardware logic chip includes at least one field programmable gate array (FPGA) chip.

4. The system of claim 3, wherein the clock generation logic includes:

a plurality of clock generation slices for generating a plurality of clocks, where each clock generation slice generates a clock in response to a trigger signal; and

a clock scheduler for generating the trigger signal to the plurality of clock generation slices so that the generation of the clocks by the plurality of clock generation slices is scheduled in accordance with the desired phase relationships among the plurality of clocks.

5. The system of claim 4, wherein the clock scheduler further comprises:

toggle point logic for determining a next toggle point among the plurality of clocks; and

trigger logic for generating the trigger signal for the clock associated with the next toggle point.

6. The system of claim 4, wherein each of the plurality of clock generation slices further comprises:

toggle generation logic for toggling a logic state of the clock associated with the clock

generation slice in response to a toggle signal; and

toggle signal generation logic for generating the toggle signal if the time duration from the current time to the next toggle point among the plurality of clock generation slices is the lowest.

7. The system of claim 1, further comprising:

a target system for receiving a first data from the evaluation logic and delivering a second data to the evaluation logic, wherein the target system is controlled by the plurality of asynchronous clocks generated by the clock generation logic.

8. A clock generation logic system for generating a plurality of asynchronous clocks, comprising:

a plurality of clock generation slices for generating a plurality of clocks, where each clock generation slice generates a clock in response to a trigger signal; and

a clock scheduler for generating the trigger signal to the plurality of clock generation slices so that the generation of the clocks by the plurality of clock generation slices is scheduled in accordance with the desired phase relationships among the plurality of clocks.

9. The system of claim 8, wherein the clock scheduler further comprises:

toggle point logic for determining a next toggle point among the plurality of clocks; and

trigger logic for generating the trigger signal for the clock associated with the next toggle point.

10. The system of claim 8, wherein each of the plurality of clock generation slices further comprises:

toggle generation logic for toggling a logic state of the clock associated with the clock generation slice in response to a toggle signal; and

toggle signal generation logic for generating the toggle signal if the time duration from the current time to the next toggle point among the plurality of clock generation slices is the lowest.

11. A method of verifying the proper operation of a user design, comprising steps:

providing a hardware model of the user design among a plurality of reconfigurable chips;

generating a plurality of asynchronous clocks for driving the hardware model;

providing input data to the hardware model for evaluation during an evaluation period; and

controlling the phase relationship among the plurality of asynchronous clocks during the evaluation period.

12. The method of claim 11, wherein the step of controlling further comprises steps:

determining a current time;

determining a next toggle point from among the plurality of asynchronous clocks from the current time; and

toggling the clock associated with the next toggle point.

13. The method of claim 12, further comprising step:

updating the current time with the time associated with this next toggle point; and

determining a new next toggle point from among the plurality of asynchronous clocks from the updated current time.

14. The method of claim 12, wherein the step of determining the next toggle point further comprises:

determining a time duration from the current time to the next toggle point for each of the plurality of asynchronous clocks; and

selecting the lowest time duration from among the time durations of the plurality of asynchronous clocks.

15. A method of generating a plurality of asynchronous clocks, where each clock includes a plurality of toggle points and a toggle point represents a point in time where the logic state of the clock changes, comprising steps:

determining a first current time;

determining a first time duration from the first current time to each clock's next toggle point;

comparing each clock's respective first time durations;

selecting the clock associated with the lowest value among the first time durations; and

toggling the logic state of the selected clock.

16. The method of claim 15, further comprising steps:

updating the first current time with a second current time where the second current time is the time associated with this next toggle point; and

determining an adjusted time duration from the updated current time to each clock's next toggle point.

17. The method of claim 16, wherein the step of determining the adjusted time duration includes:

determining a differential time duration from the first current time to the second current time; and

subtracting the differential time duration from each unselected clock's respective first time duration to generate the adjusted time duration.

18. The method of claim 17, further comprising steps:

determining a second next toggle point for the selected clock; and

determining a second time duration from the second current time to the second next toggle point.

19. The method of claim 18, further comprising steps:

comparing the adjusted time duration of each of the nonselected clocks and the second time duration of the selected clock; and

selecting the clock associated with the lowest of any of the adjusted time durations and the second time duration.

20. The method of claim 19, further comprising step:

toggling the logic state of the selected clock.